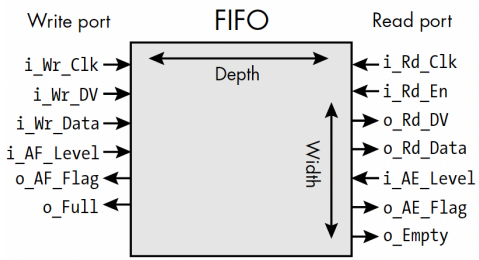
Getting Started with FPGAs

Digital Circuit Design, Verilog, and VHDL for Beginners

by Russell Merrick

errata updated to print 2

Page	Error	Correction	Print corrected
17	4. **As the software is downloading, find the iCECube2 Software Free License link on the download page and click it to request a license.**	4. **You'll need to request a license, which is free for hobbyists and similar users but can take a couple days to arrive in an email. Follow the steps in the "Licensing" section of the iCEcube2 page to start the process.**	Print 2
18	1. Go to ***https://latticesemi.com/programmer*** or search the internet for "lattice diamond software" to locate the download page. 2. The **Diamond Programmer page** has many download links to choose from. Find and click the link for the latest version of Programmer Standalone 64-bit for Windows. **WARNING** Be sure to download Programmer Standalone and not the Programmer Standalone Encryption Pack. The latter isn't needed.	1. Go to ***https://www.latticesemi.com/diamond*** or search the internet for "lattice diamond software" to locate the download page. 2. The **Software Downloads section** has many download links to choose from. Find and click the link for the latest version of Programmer Standalone 64-bit for Windows. **WARNING** Be sure to download Programmer Standalone and not the **Diamond or** Programmer Standalone Encryption Pack. The latter isn't needed.	Print 2
26	The final step in the process is to program your design to your FPGA using Diamond Programmer.	The final step in the process is to program your design to your FPGA using Diamond Programmer **(from the Programmer Standalone download earlier)**.	Print 2
38	It also occurs on the **fifth** line of the truth table, so we can fill those in with a 1.	It also occurs on the **sixth** line of the truth table, so we can fill those in with a 1.	Print 2
117	Figure replacement	 *Figure 6-9: A detailed FIFO block diagram*	Print 2
117	On the read side, the `i_Rd_En` and `i_Rd_DV` signals similarly communicate when we wish to read data . . .	On the read side, the `i_Rd_En` and `o_Rd_DV` signals similarly communicate when we wish to read data . . .	Print 2
118	If the number of elements (sometimes called *words*) in the FIFO is **greater than or equal to the value set by** `i_AF_Level`, then `o_AF_Flag` will be high.	If the number of elements (sometimes called *words*) in the FIFO is **such that** `i_AF_Level` **more words will not fit**, then `o_AF_Flag` will be high.	Print 2

Page	Error	Correction	Print corrected
118	To prevent data loss, we would want to set `i_AF_Level` to ***depth*** **– 4** and then check that `o_AF_Flag` is low before writing each burst of four elements.	To prevent data loss, we would want to set `i_AF_Level` to **4** and then check that `o_AF_Flag` is low before writing each burst of four elements.	Print 2
119	Deletion	~~Remember that `o_AE_Flag` is set when the count is less than or equal to `i_AE_Level`.~~	Print 2
119	All flags are low from words five through seven, but when there are eight words in the FIFO, `o_AF_Flag` goes high (since `i_AF_Level` was set to **8**).	All flags are low from words five through seven, but when there are eight words in the FIFO, `o_AF_Flag` goes high (since `i_AF_Level` was set to **5, and 12 – 5 = 7**). **Said another way, we don't have enough space for 5 more words when the count is at 8.**	Print 2
174 (ebook only)	When this happens we transition to the **`PATTERN _SHOW`** . . .	When this happens we transition to the **`PATTERN_SHOW`** . . .	Print 2
208 (ebook only)	For example, 100010 100 becomes 011101 100.	For example, 100010**100** becomes 011101**100**.	Print 2
Back cover	The book I wish had	The book I wish **I** had	Print 2